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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/754,860	01/04/2001	Robert S. Mason JR.	EMS-01401	3989

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EXAMINER	
MCLEAN-MAYO, KIMBERLY N	

ART UNIT	PAPER NUMBER
2187	12

DATE MAILED: 05/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	09/754,860	MASON ET AL.	
	Examiner	Art Unit	
	Kimberly N. McLean-Mayo	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 February 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The enclosed detailed action is in response to the Amendment submitted on February 25, 2003.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 4-5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claim 4 recites the limitation "the section" in line 2. There is insufficient antecedent basis for this limitation in the claim.
Claim recites a first section and a second section, therefore, it is not clear which section "the section" refers to.

5. Claim 5 recites the limitation "the section" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

7. Claims 1 and 8-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamamoto et al. (USPN: 6,408,370).

Regarding claim 1, Yamamoto discloses a data storage system comprising a first disk drive unit (Figure 1, comprised of References 109 and 105); a second disk drive unit, coupled to the first disk drive by a bus (Figure 1, comprised of References 104 and 105); a main cache memory, coupled to the bus, that caches data from at least one of the first disk drive unit and the second disk drive unit (Figure 1, Reference 108 within Reference 104); a secondary memory separate from the main cache memory (comprised of References 107,108 within Reference 109) and provided as part of the first disk drive unit, wherein the secondary memory has at least two sections, a first section used by the first disk drive unit to facilitate disk accesses (Figure 1, Reference 107 within Reference 109; control memory; C 4, L 60-66; the information within the first section of the secondary memory used to facilitate disk accesses is described in C 4, L 14-59) and a second section (Figure 1, Reference 108 within Reference 109) used to cache data

provided to the second section from the second disk drive unit (C 5, L 28-36, L 53-55 – the second disk drive unit provides data, via Reference 104, to the second section of the secondary memory).

Regarding claim 8, Yamamoto discloses a first disk drive including a section of onboard memory (Figure 1, onboard memory comprised of References 108 and 107 within Reference 109) associated with the first disk drive (first disk drive is comprised of References 105 and 109 in Figure 1) and including an interface that handles data communication to and from the first disk drive (inherent – the disk drive control unit comprises internal elements which receive inputs and outputs data thereby handling data communication to and from the disk drive); a second disk drive that provides data to the first disk (the second disk drive is comprised of References 104 and 105 in Figure 1; C 5, L 28-30); memory for caching data of the data storage system (Figure 1, memory is comprised of References 108 and 107 within Reference 109 and Reference 108 within Reference 104), the memory including the section of onboard memory associated with the first disk drive wherein the section includes a portion of data cached from at least the second disk drive and wherein data from the second disk drive is provided to the onboard memory (C 5, L 28-36, L 53-55 - the second disk drive provides data, via Reference 104, to the section of onboard memory).

Regarding claim 9, Yamamoto discloses the onboard memory including a portion of data that is not duplicated elsewhere in the data storage system (Figure 1, Reference 107).

Regarding claim 10, Yamamoto discloses the onboard memory including a portion of data that is duplicated elsewhere in the data storage system (Figure 1, Reference 108).

Regarding claim 11 and 18, Yamamoto discloses the memory for caching including a portion of system memory of the data storage system (inherent – the data storage system is an extension of the system memory and thus is also system memory and therefore, data caching, via the cache[also the system memory cache], for the data storage system, inherently caches data of the system memory).

Regarding claim 12, Yamamoto discloses a command generator (comprised of processing unit 100 and unit 140 in Figure 1) that generates at least one command for performing a data operation in connection with caching data of the system memory and at least one command for performing a data operation in connection with caching data of the section of onboard memory (the processing unit stores data in the system memory, 102, when data is retrieved from 105, thereby caching data of the system memory, since the data storage device is an extension of the system memory; and unit 140 writes data to Reference 109, wherein the data is cached in Reference 108 within Reference 109; C 5, L 28-55).

Regarding claim 13, Yamamoto discloses a first command generator (Figure 1, Reference 104 – control logic/software within Reference 104 which operates cache, Reference 108) that generates at least one command for performing a data operation in connection with caching data of the system memory (C 5, L 9-21; data to be written to the data storage system is stored in cache 108,

the data storage system is an extension of the system memory and thus the cache caches data of the system memory); and a second command generator (Figure 1, Reference 109 - control logic/software within Reference 109 which operates cache, Reference 108) different from the first command generator that generates at least one command for performing a data operation in connection with caching data of the section of onboard memory (C 5, L 28-55).

Regarding claim 14, Yamamoto discloses a command generator (Figure 1, Reference 109 - control logic/software within Reference 109 which operates cache Reference 108) that generates at least one command for performing a data operation in connection with data caching of the section of onboard memory (C 5, L 28-30).

Regarding claims 15-17, Yamamoto discloses a host interface unit that includes the command generator (Figure 1, logic within Reference 104 which couples to the host processor(s)), wherein the command generator executes on a dedicated processor (the controller, which comprises the command generator, is a dedicated specialized processor and thus the command generator executes on a dedicated processor), the host interface unit being connected to a host computer (the controller is coupled to the host(s) via channel 103); a disk interface unit for interfacing with the first disk drive (Figure 1, logic within Reference 104 which interfaces to disk drive 105).

Regarding claim 19, Yamamoto discloses a command interpreter that interprets commands in connection with a data caching operation of at least one of the section of onboard memory and

the system cache memory (Figure 1, Reference 109 – logic within Reference 109 that receives and executes commands).

8. Claim 2 is rejected under 35 U.S.C. 102(e) as being anticipated by DeKoning et al. (USPN: 6,381,674).

DeKoning discloses a disk drive unit (the disk drive unit is comprised of References 412, 414, one of References 416, one of References 404, References 406, 408, 410 and 418 in Figure 4), comprising an interface that communicates data to and from the disk drive unit (Figure 4, References 412 and 414); a first disk platter that stores data (the first disk platter is comprised of the one of References 416 in Figure 4 comprised in the disk drive unit); and a controller coupled to the interface and the first disk platter (the controller is comprised of one of References 404 comprised in the disk drive unit, and References 406 and 408 in Figure 4), the controller providing and accepting data signals that control the disk drive unit and communicate data therewith (C 15, L 15-67; C 16, entire; C 17, entire – the controller accepts signals, such as signals to perform read/write requests, from the host via Reference 404, refer to C 15, L 30-34, L 58-60, and provides signals to the disk platter, such as signals to perform read/write requests when a cache miss occurs, via Reference 404, refer to C 16, L 55-59), wherein the controller includes a memory (Figure 4, Reference 410 within References 406 and 408) having a first portion that is useable as cache for data that is stored on the first disk platter (Figure 4, Reference 410 in Reference 406; C 11, L 3-15; cache, 410, stores data from a first half of the storage elements including the first disk platter) and having a second portion that is useable as cache for data that is stored on a second disk platter that is separate from the disk drive unit (the second

disk platter is comprised of a different one of References 416 in Figure 4) (the second portion of the memory is comprised of Reference 410 in Reference 408 in Figure 4; C 11, L 3-15; cache, 410, stores data that is in a second half of the storage elements including the second disk platter), wherein the second portion is provided with data from the second disk platter (Figure 6, Reference 606, 608, 610 and 612 – data from the second disk platter is provided to the second portion of the memory when a cache miss occurs).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 3-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto (USPN: 6,408,370).

Regarding claim 3, Yamamoto discloses a first section of onboard memory containing data for the storage device (Figure 1, Reference 107 within Reference 109; control memory; C 4, L 60-66; the data within the first section of the memory for the storage device is described in C 4, L 14-59) and a second section of onboard memory associated with the data storage device and used as a cache including data cached from at least one other data storage device, wherein the second section of onboard memory is provided with data from the at least one other data storage device (Figure 1, Reference 108 within Reference 109; C 5, L 11-13, L 28-36, L 53-55 – the at least one other storage device provides data, via Reference 104, to the second section of onboard

memory). Yamamoto does not disclose the onboard memory as a volatile memory. The onboard memory in Yamamoto's system is a nonvolatile memory. It is well known in the art to use volatile memory to store data. It is also well known in the art the nonvolatile memory requires data to be erased before overwritten which increases latency, whereas volatile memory can be overwritten without first erasing. Hence, one of ordinary skill in the art would have recognized the benefits afforded by a volatile memory such as reduced latency and would have been motivated to use a volatile memory in Yamamoto's system for the desirable purpose of decreased latency.

Regarding claims 4-5, Yamamoto discloses the data storage device as a first disk drive unit (Figure 1, Reference 109 and 105) and the onboard volatile memory includes data cached from at least a second disk drive unit (C 5, L 28-36, L 53-55) and from the first disk drive unit (the first disk drive unit stores data, received by the second disk drive unit, in the onboard memory).

Regarding claims 6-7, Yamamoto discloses an interface that provides and accepts data (inherent – the disk drive control unit, Reference 109 in Figure 1, comprises internal elements which receive inputs and outputs data) and a disk platter that stores data (Figure 1, Reference 105); and a controller that handles communication between the interface and the disk platter, wherein the onboard volatile memory is part of the controller (Figure 1, Reference 109 – internal logic within Reference 109 that handles communication between the interface and the disk platter); a processor of the data storage device (processing element within Reference 109); an other section of onboard volatile memory associated with the data storage device wherein the processor uses

the other section of onboard volatile memory in connection with accessing data stored on the disk platter (Figure 1, Reference 107 within Reference 109; control memory; C 4, L 60-66; the data within the first section of the memory for the storage device is described in C 4, L 14-59).

Response to Arguments

11. Applicant's arguments filed February 25, 2003 have been fully considered but they are not persuasive.

Regarding Applicant's argument, with respect to claim 1, that Yamamoto discloses data from the processor written to at least one of the memories but does not show, teach or suggest any data from one of the disk drive units coupled to the controllers being provided from the disk drive unit to the memory of the other one of the controllers, the Examiner disagrees. The Applicant's arguments are inconsistent with the rejection. The above rejection states that the first disk drive unit is comprised of References 109 **and** 105 in Figure 1 and that the second disk drive unit is comprised of References 104 **and** 105 in Figure 1, wherein the second disk drive unit provides data **via Reference 104** to the second section of memory . Accordingly, Yamamoto teaches the claimed limitations.

Applicant's arguments with respect to claim 2 have been considered but are moot in view of the new ground of rejection.

Regarding Applicant's arguments with respect to claim 8, the Applicant has again provided arguments that are inconsistent with the rejection. Yamamoto teaches the recited memory,

Figure 1, memory is comprised of References 108 and 107 within Reference 109 and Reference 108 within Reference 104, that includes the section of onboard memory, Figure 1, onboard memory comprised of References 108 and 107 within Reference 109, associated with the first disk drive, which is comprised of References 109 **and** 105 in Figure 1, where the section includes a portion of data cached from at least the second disk drive, which is comprised of References 104 **and** 105 in Figure 1, and where data from the second disk drive is provided to the onboard memory (C 5, L 28-36, L 53-55 – the second disk drive unit provides data, via Reference 104, to the second section of the secondary memory).

Regarding Applicant's arguments regarding claim 3, the Examiner disagrees. The above rejection describes how the prior art teaches the claimed limitations.

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

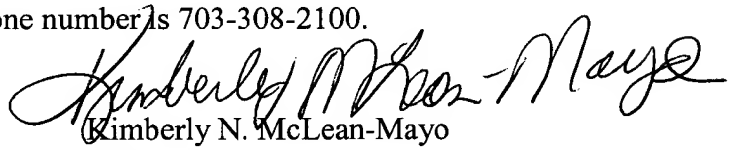
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimberly N. McLean-Mayo whose telephone number is 703-308-9592. The examiner can normally be reached on M-F (9:00 - 6:30) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 703-308-1756. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7329 for regular communications and 703-746-7240 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-2100.



Kimberly N. McLean-Mayo
Examiner
Art Unit 2187

KNM

April 25, 2003